Hardness Assurance and Testing Techniques for High Resolution (12- to 16-bit) Analog-to-Digital Converters*

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Abstract

This paper discusses hardness assurance and testing techniques to test and evaluate total dose radiation degradation of high resolution A/D converters. A 16-bit converter with internal calibration is compared with older designs (12-/14-bit) that use more conventional architectures. The results show that measurements of dc parameters and static linearity at major code transitions should be adequate for hardness assurance testing, with considerable cost savings compared to full dynamic or all-codes testing.

The failure level of CMOS and BiCMOS converters depends on dose rate in a complicated way that is not adequately addressed by high-temperature annealing. Tests at low dose rates -below 0.01 rad(Si)/s- are recommended for space applications of these technologies.

1. Introduction

During the last two years, total dose radiation tests have been done on several analog-to-digital converters (ADCs) from different manufacturers. Because high-speed. High-resolution converters are critical parts in a digital signal processing or data acquisition system, the evaluation of performance in the early design phase is very important. Electrical characterization testing set-up for these devices is complex and time consuming, and requires expensive high-speed mixed-signal test systems with extremely low noise and high sensitivity. For example, the dynamic range of a 16-bit converter is between 100-120 dB and must resolve voltages below 100 μV. Setting-up an electrical characterization test system with a noise floor below this level is a challenging effort.

This paper discusses techniques to test and evaluate total dose radiation damage in high-resolution successive-approximation converters that eliminate the need to test each individual bit or transition. Various approaches were compared to see if simplification could be made. By selecting critical parametric measurements, based on internal failure mechanisms, it is possible to develop a simplified test approach that will provide a good approximation of the converter response for total dose radiation evaluations and significantly reduce testing costs.

11. Device Descriptions

A/D converters from three different manufacturers are discussed in this paper. They are designed and fabricated with commercial CMOS or BiCMOS processes that do not take radiation hardness into account. The 16-bit converter was designed by Crystal Semiconductor, the 14-bit converter is from Analog Devices, and the 12-bit converters were manufactured by Maxim. All three devices use much higher power supply voltages than digital CMOS, and consequently they have much thicker gate oxides, which adversely affects their radiation hardness [1]

As converter designs have evolved to increase resolution, speed, and accuracy, their radiation tolerance has diminished. The total dose radiation failure level for 12-bit converters was about 6 krad(Si), the 14-bit converter was about 4 krad(Si), and the 16-bit converter was ? krad(Si). The reason for decreased radiation tolerance appears to be related to the increased complexity of internal circuitry that is needed to increase performance and accuracy, not fundamental differences in the radiation response of internal components.

Even though newer designs have much smaller steps between successive bits, the failure modes are generally more global, and can be determined without the extreme accuracy required to detect single LSB errors or minor deviations in the transfer characteristics. However, in addition to parametric tests, it is also important to check the converter functionality. This must be done over the entire voltage range, because some failure modes may affect the linearity and range only near the extremes of the specified input range.

Each converter has its own characteristics to fit various circuit applications and provides flexibility for design applications. The three converters use different architectures. The 16-bit device is an unusual design that uses an internal microprocessor and error register to provide self-calibration of first-order

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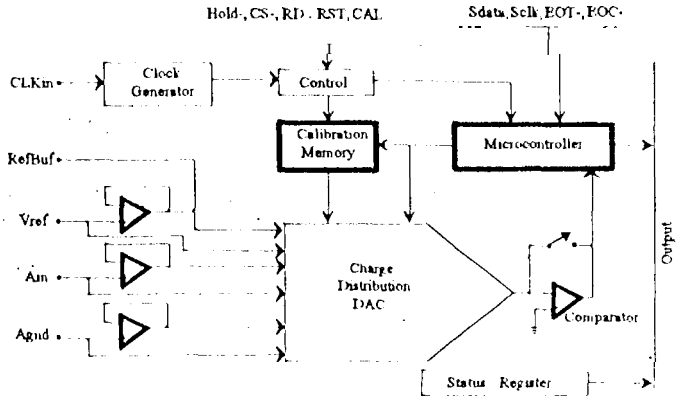


Figure 1. CS5016 Functional Block Diagram [2]

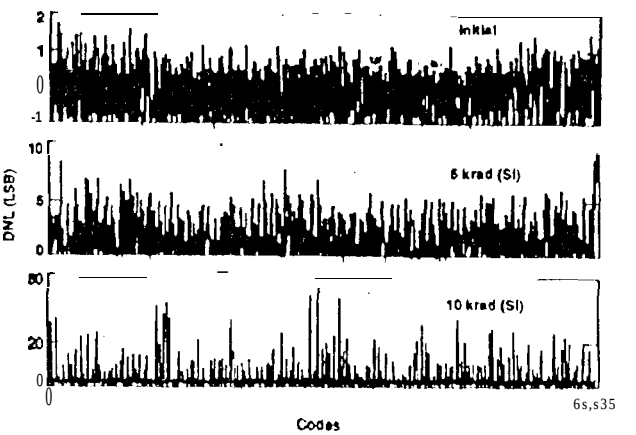


Figure 2. DNL Degradation of 16-bit A/D Converter

inaccuracies. A simplified functional block diagram is shown in Figure 1, In addition to the microcontroller and calibration circuits, this device uses a switched-capacitor digital-to-analog converter (DAC). Although one would expect this approach to improve total dose r-ad ation hardness, this device washy far the most sensitive to total dose degradation. One reason is the use of internal buffer amplifiers at the reference, analog input, and ground input terminals. These CMOS amplifiers degraded very rapidly at low total dose levels.

The AD7872 is a BiCMOS 14-bit successive-approximation ADC that consists of a fast-settling output DAC, a high-speed comparator, CMOS SAR, a track/hold amplifier, an internal reference, a clock oscillator, and control logic.

The 1 2-bit converters have an internal reference voltage and clock along with conventional digital subfunctions such as SAR. control and timing logic. They arc also fabricated with a BiCMOS process.

Testing Techniques anti Test Results

Total dose irradiations were done with a Shepherd ^{60}Co room type irradiator with a source strength of 10 kCuries for high dose rate testing. A similar ^{60}Co source with less intensity was used for low dose-rate irradiations. Dose rates as low as 0.002 rad(Si)/s were used for some of the. irradiations. All test devices were statical ly biased during irradiation Several different test methods were used to determine overall performance characteristics, including integral nonlinearity (INL) and differential nonlinearity (DNL). Static and dynamic test methods were compared for the 14-bit and 16-bit converters.

16-bit ADC (CS5016)

The Crystal Semiconductor CS501616-bit A/D converter is fabricated with a 3 µm CMOS process with a total power supply voltage of 10 V. The analog input range is only 4 .S V in unipolar mode resulting in an LSB of 68,7 µV, an extremely small voltage. As discussed previously, it uses a witched. capacitor-based architect ure, with internal microprocessor control and error calibration Most other converters use a conventional architecture with laser-trinmmd thin-film technology and a ladder network based on current sources.

Despite the internal self-calibration circuitry, the 16-bit converter failed parametrically at very low total dose levels - ≈5 krad(Si)– when tested at a high dose rate of 50 rad(Si)/sec. Converters recovered both functionally and parametrically during a 168 hours room temperat ure annealing test after they were irradiated to 20 krad(Si) at high dose rate. They remained functional after a subsequent a high-temperature annealing test (loo “c).

Linear i ty Testing

A histogram-based test was set up to measure the converter linearity. The histogram test is a statistical method of deriving the con verter's differential nonlinearity (DNL) from AC t ests at a single frequency.[3] A spectrally pure sinewave along with an active low-pass filter was applied at the input of the converter. Only one million samples were taken to limit the test time period, but it provided enough infor mat ion about the 16-bit converter performance. In this test, a code with more or less occurrences than average appears as a DNL greater or less than zero LSB; the top trace in Figure 2 shows typical results before irradiation

Using this approach, DNL failed below 5 krad(Si) as shown by the large number of missing codes after 5 krad(Si) in the middle waveform of Figure 2 (Note the different scales for the three histograms in the figure). At higher radiation levels, large variations occurred in the frequency distribution including several missing. codes, and partial loss of functionality.

Although linearity errors are important characterization parameters, power supply current can be an effective indicator of global degradation of either the subthreshold leakage of internal CMOS transistors, or field oxide leakage. Power supply current exceeded the specification limit at 10 krad(Si) as shown

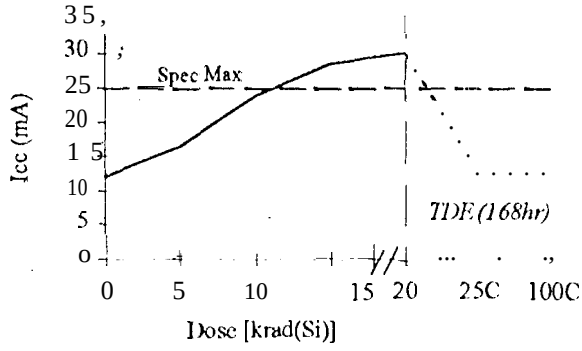


Figure 3. Power Supply Current of 16-bit A/D Converter

in Figure 3. Devices functionally failed at 15krad(Si). This data indicates that the converter is extremely vulnerable to total dose irradiation The data was taken with a test set-up using an internal clock. Note that power supply current recovered to its preirradiation value after annealing at room temperature.

Reference Voltage Testing

The reference voltage is onc of the most critical parameters because the reference voltage establishes the gain required to *meet* the highly accurat e specifications of these converters. The digital output should correspond to the ratio of the analog input signal to the reference voltage with integral and differential nonlinearity of less than 100 µV. An external reference voltage of 4.5 V is required for operation of the 16-bit converter and it passes through an int ernal CMOS buffer amplifier and fed to the internal 16-bit DAC. Even though the converter uses an external reference, changes in the buffer amplifier will affect the reference voltage at internal points within the circuit, The converter uses several CMOS buffers, and the offset of the buffer can be measured with the standard pinout of the circuit (see Figure 1),

The voltage at the output of the buffer amplifier was measured during radiation and it degraded sever ely as shown in Figure 4. Note that significant changes begin to occur at approxi mat ely 2 krad(Si), an extremely low level, and that changes of *several hundred* LSB occur at S krad(Si). This may be duet o threshold voltage changes in the buffer amplifier. The gate threshold voltage shift of MOS devices is the dominant total dose radiation problems, [1] Similar buffer amplifiers arc used in the analog input and analog ground paths,

Once an external reference voltage is applied to the converter, internal capacitors in the calibrated capacitor army of the converter switch from the reference voltage to the analog ground level, due to the SAR algorithm. 'he same CMOS amplifier is used in the internal analog input, analog ground, and comparator circuitry. The internal comparator 'connects a critical path between the output of the internal DAC and the microcontroller. Degradation in the reference buffer amplifier indicates that the other buffer circuits will behave the same way under total dose irradiation. Because of the internal calibration, the CS5016 can tolerate significant changes in the reference voltage, }low'ever. the results in Figure 2 show that the complex architecture is not capable of correcting for changes exceeding approximately 50 LSB.

FFT Testing

The converter was tested using Fast Fourier Transform (FFT) techniques to analyze the dynamic performance and measure SNR and THD parameters. Figure 5 shows magnitude spectrum test results at a high dose rate (50 rad(Si)/s) lest. The noise floor level and the distortion of the harmonics increased tremendously at 20 krad(Si). This is there.suit of the increase in the converter noise duc to irradiation,

Tests at very low dose rate (0.005 rad(Si)/s) showed that converters sur vived much higher radiation level compared to the high dose rate test results. The SNR started to degrade slightly at 9 krad(Si) to 88 dB which is the minimum specification limit, the initial SNR value was 91.S dB. However, no other significant degradations were observed to the final total dose level of 20 krad(Si).

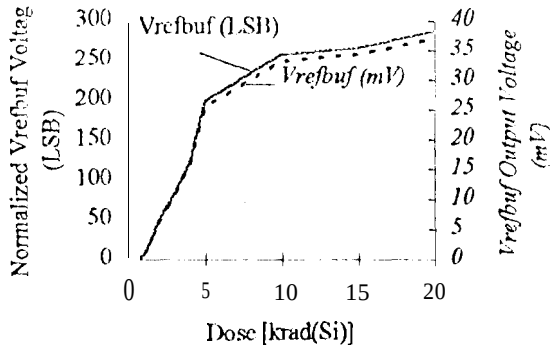


Figure 4. Vrcf Buffer Output Voltage Degradation of 16-bit A/D Converter

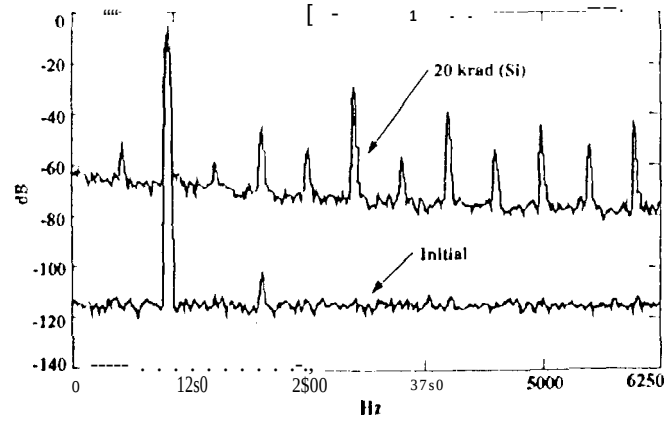


Figure S. CS501616-bit ADC Magnitude Spectrum

Dynamic tests were performed with internal and external clocIM. The FFT test to measure SNR/THD parameters did not work properly with the internal clock because there was too much jitter. Because calibration, conversion time, and data throughput time are directly scaled with the clock signal, any noise or disturbance in the clock will induce conversion errors. The manufacturer stated that the internal oscillator of the converter would vary from device-to-device and over temperature. Thus, converter conversion can be more precisely controlled using an external clock signal rather than the marginally stable internal clock, Therefore the converters were tested with only the external clock mode for total dose radiation.

This unique self-calibration converter showed failures at low total dose levels due to the sensitivity of CMOS devices under total dose irradiation. Commercially processed CMOS devices have the dominant total dose radiation problems failing at low dose levels with the high dose rate test. 1 however, converters showed much higher failure levels with the very low dose rate test, consistent with the expected annealing behavior of these devices. [1]

B. 14-bit ADC (AD7872)

Analog 1 Devices AD7872 is a 14-bit A/D converter, fabricated in Bi CMOS technology. It uses a conventional architecture, with a comparator, internal reference, and successive-approximation register (SAR) using a current-switch ladder network. It operates with the power supply voltage of ±5V and a ±3V input signal is required.

High Dose Rate Tests

This device uses a laser-trimmed oscillator as an internal clock Converters were equally functional with an internal clock and an external clock prior to irradiation. However, the radiation failure level of the device had an unusual dependence on the clock mode. Total dose test data with a dose rate of 50 rad(Si)/s. a high dose rate, showed that SNR and functional tests failed at 4 krad(Si) using an external clock. When the internal clock was used, failure did not occur until 40 krad(Si) as shown in Figure 6. These test results show that the total dose response can vary substantially with different operating modes. The functional failure level of the converter can be improved signi -

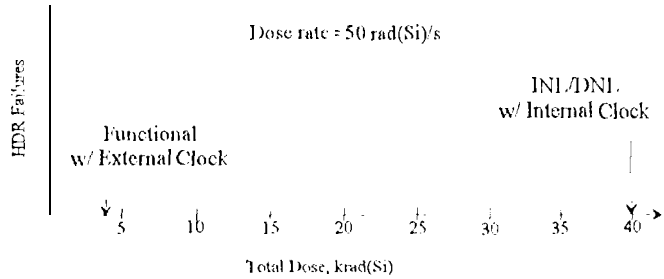


Figure 6. AD7872 HDR Test Results

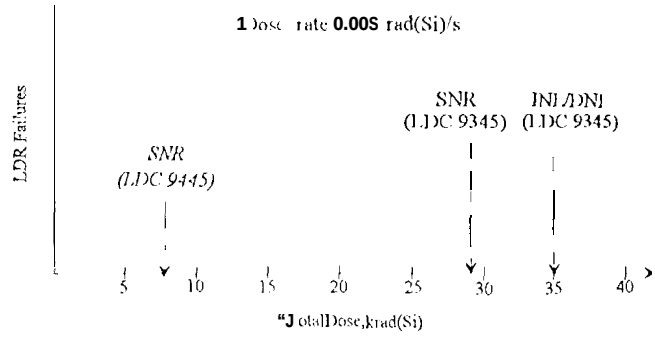


Figure 7. AD7872 LDR Test Results

cantly, an order of magnitude, using the internal clock rather than the external clock in a circuit application.

The external clock bypasses the last? trimmed internal clock oscillator, connecting the output of the clock circuit directly with the internal CMOS comparator. The input circuitry of the external clock input of the converter uses a CMOS analog switch to bypass the internal clock. The on-characteri - tics of CMOS switches are often highly sensitive to radiation degradation, which may explain the large difference in the circuit hardness with different clock modes.

Low Dose Rate Tests

Very low dose rate (0.005 rad(Si)/s) test results for older date code devices (LDC 9345) showed that converters were fully functional with no significant parametric degradations up to a total dose level of 29 krad(Si). SNR dropped 2 dB below the minimum specification limit of 80 dB after the highest levels.

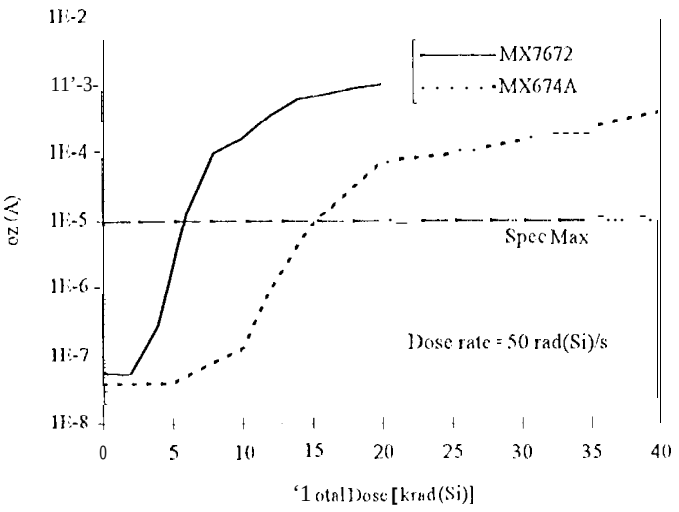
Much different results occurred for a newer date code from this same manufacturer (LDC 9445) when it was tested at low dose rate. As shown in Figure 7, SNR started to degrade at 7.5 krad(Si). The internal and external clock modes did not introduce any different failures during low dose rate testing. The reference voltage did not show any degradation until 35 krad(Si) where the linearity started to degrade.

C. 12-bit ADC (MX7672/MX674A)

These devices are also fabricated with BiCMOS processes, and use a conventional architecture. The CMOS devices have thick gate oxides because of the 18 V voltage rating of these parts. The MX674A has an internal reference voltage, which exceeded the specification limit at relatively low total dose levels. Otherwise, the response of the two devices were very similar.

High Dose Rate Tests

Tri-state leakage current, Ioz, is one of the most important dc parameters and it failed at low levels of radiation when tests were done at high dose rate. These failures are caused by



Figur c 8. loz Degradation of 12-bit BiCMOS ADCs

subthreshold leakage curr ent in MOS transistors in the output stage, which increases clue to radiation.

The loz parametric failure is caused by oxide traps in the output transistors for these Bi CMOS devices. The increase in loz with devices statically biased during the high dose ralc radiation test is shown in the Figure 8. The r apid recovery during an annealing time period at room temperature indicates that the total dose hardness is strongly affected by the dose rate. [4]

Low Dose Rate. Tests

At an intermediate dose rate (0.01 rad(Si)/s), loz no longer dominated the radiation behavior which is consistent with the internal failure mechanism and the annealing results after tests at high dose rate. Low dose rate test results showed that the linearity of the MX7672 converter failed at 11 krad(Si); INL and DNL d i d not chat ige significantly at high d o s e rates until approximately 20 krad(Si).

DC parameters including loz showed some degradation at 11 krad(Si), but all were within specification limits. loz started exceed the specification limits at 13 krad(Si). '1'bus, at interme-diate dose I-ate. linearity degradation dominates the device response.

At lower dose rates, these converters fail edcatastrophi tally at very low total dose 1 evels. At 0.002 rad(Si)/s, catastrophic failure occurred at approximately 7 krad(Si); the catastrophic failure level increased to ≈12 krad(Si) al 0.005 rad(Si)/s. The catastrophic failure is assumed to be caused by MOS threshold shift, and probably occurs because of net positive shifts due to rebound. Once catastrophic failure occurred some outputs were stuck high. Annealing, at mom temperature did not affect the stuck bits.

Table]. Hardness Comparison of Technology

Devic :	Tech	Power Supply Voltage Range	LSB
CS5016 (16-11,1)	CMOS	10V	68.7uV
AD7872 (14-bit)	BiCMOS	10V	366 n\'
MX7672 (12-111[)	BiCMOS	17V	2.44mV

IV. Hardness Assurance Techniques

.4. *Process Technology*

Hardness assurance testing requires a trade-off between electrical testing and lengthy irradiations, so that testing cost and time must be reduced as much as possible. Initially it would appear- that the range of the input voltage would be the major factor for sensitivity of the linearity failures in ADC operation, but the process technology d ifferences, CMOS vs. BiCMOS, were more critical during radiation hardness assurance tests. "1'able I summarizes the results of the total dose testing for both technologies.

The extreme sensitivity of the CMOS process may y be due to the difficulty of designing linear amplifiers with low offset voltage, compared to BiCMOS processes, which use bipolar transistor s that ar e inher ently better matched than CMOS. [5]

B. Measuremer nt Selection

Tremendous effort is required in order to test a high-resolution and lligJ}-speed ADC for full specifications. For example, setting up a SNR test, dynamic parameter test for 16-bit ADC s with small input range is very difficult because the noise floor should bc at around -120 dB. In contrast, d c parameters such as Icc, loz, Vref, and Voh/Vol along with a static functional test can be easily set up and measured with a digital test system with a precise analog signal source. Figure 9 shows the approximate relationship bctw'cell cost and difficulty of the test setup of ADCs The measurem ent set-up for stati c linearity parameters can be limited to regions near transition codes and can be achieved without expensive test equipment.

The cost of a static test would be only the fraction of the dynamic parametric testing. A histogram test is required for the dynamic linearity test A FFT test set-up for SNR measurem ent is very difficult and noise is the major problem. This dynamic test set-up not only requires delicate equipment and expensive precision test systems but also requires time consuming prepa-ration.

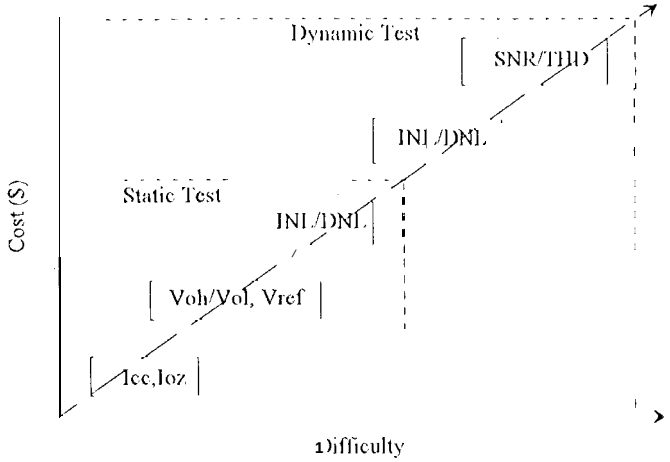


Figure 9. Selection of Parametric Measurements

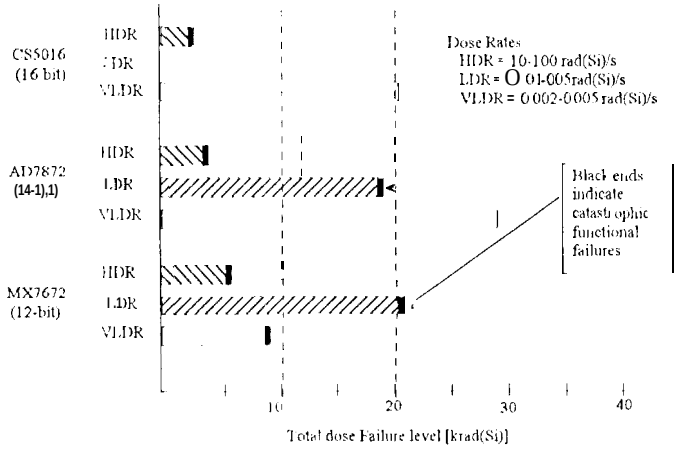


Figure 11. Dose Rate Dependence of ADCs

Our tests of 14-bit and 16-bit converters included static and full dynamic tests; these results were discussed earlier-. For both converters the radiation failure mode did not depend cm the testing mode, except for noise, which can be evaluated without full dynamic testing. This suggests that a static testing approach, evaluating INI, and DNL near each major transition, will be adequate for radiation tests.

C. *Lot Variability*

Lot-to-lot variations in the results of radiation testing are clearly important for hardness assurance. Substantial difference in hardness occurred for different dale codes of the 14-bit and 16-bit converters. For the 16-bit converter, the older dat c code devices per-formed better initially and also due to total dose radiation. For the 14-bit ADC, AD7872, the later date code failed parametrically at a lower total dose level. Figure 10 shows SNR degradation of two different lot dale codes of the 16-bit coil\'cl"fcl".

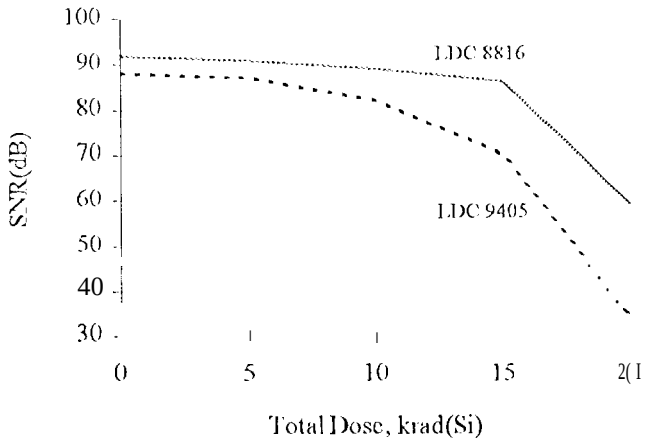


Figure 10. SNR Degradation of 16-bit ADCs from Two Different Date Codes

D. *Dose Rate Selection*

The 14-bit and 16-bit converters showed significant improvement of the total dose failure level at the very low dose rate of 0.002-0.005 rad(Si)/s compared to the low dose rate and the high dose rate as shown in Figure 11. The advantage of the very low dose rate testing is that the degradation will be less and the total dose failure level can be much higher. However, the very low dose rate total dose testing will take much longer time period to complete.

Although alternative techniques have been developed for hardness assurance in digital CMOS dc]'ices that use high-temperature annealing after high dose rate testing to avoid the need to test at low dose rate tests, these techniques are risky for A/D converters. Three factors must be considered: First, the temperature used for rebound testing must be carefully selected in order to make sure that all of the holes recover, and that no interface traps anneal. A/D converters depend crit i tally on small mismatches in internal components, and will likely be more sensitive to small differences between high-temperature annealing and low dose rate damage. Secon cl, these are complex devices with several possible failure modes. The degradation is often highly nonlinear with closc, which makes it difficult to interpret the results of a rebound test. Finally, BiCMOS converters contain bipolar as well as CMOS structures, and the high-temperature rebound test has not been shown to be effective for bipolar devices. In addition, some bipolar devices exhibit close-ralr. effects. that would not be properly simulated by high-temperature rebound testing. ~'bus, low dose rate testing is the preferred approach for present technology A/D converters.

E. *Internal/External Clock Selection*

An investigation was conducted with the CMOS 16-bit ADC to evaluate differences in device performance with internal and external clocks. Initially SNR of 91dB could be measured

with the external clock. However, with the internal clock SNR was only 69 dB, which was below the specification limit (88dB). This was due to jitter in the internal clock, Despite internal calibration circuits, the noise of the internal clock made the measurement of the SNR of devices impossible.

The 14-bit BiCMOS converter, AD7872pcl-formed equally with internal and external clocks during prc-electrical characterization tests. Therefore, total dose radiation testing was conducted on the converter using both clock modes. Significant degradation differences were observed with internal and external clock modes, 4 krad(Si) with external clock and 40 krad(Si) with internal clock mode. As discussed earlier, this is likely due to the design used for the internal clock, which uses analog switches that are potentially very susceptible to radiation damage. Simila - differences in radiation response with internal and external clocks have been reported by Turflinger for A/D converters from advanced oxide-sidewall processes, [6]

In a circuit design application, proper selection of the clock mode can not only improve the device operational functionality but also improve the radiation failure level of devices and systems. The results also show the importance of specifying test conditions to match actual operating modes.

V. Discussion

One of the most sensitive parameters in static dc parametric testing of converters is the reference voltage. The reference voltage is directly related to linearity performance of converters. For 12-bit converters, slight changes in the slope of the transfer function curve due to reference voltage degradation were observed al low radiation levels, However, large discontinuties which represented the loss of major code transitions were often observed at higher radiation levels. Some converters have calibration circuits 10 automatically range variations of the reference voltage. The reference voltage must be stable and precise, especially for a 16-bit converter. Because of the large offset in the internal buffer amplifier due to irradiation. the reference voltage to the converter was severely degraded and caused the largest degradation in the performance characteristics.

The internal CMOS amplifier and comparator of a converter are critical components, and small changes in their characteristics can cause static and dynamic parametric failures. Leakage current and threshold voltage in CMOS amplifiers and comparators are extremely vulnerable to total dose irradiation and will directly introduce failures to the overall functionality of a converter.

Linearity errors in successive-approximation A/D converters are caused by bit weighted errors or comparator dynamic errors. [7] In a self-calibrating converter, comparator dynamic errors can also contribute to in linearity errors, if the comparator does not have enough time to settle during each bit decision making process in the successive-approximation algorithm 'The worst-case codes for comparator dynamic errors are the major transition codes, especially at the half of the full scale codes. Therefore, the largest linearity failure will be introduced at the major transition codes where the largest bit-weighted error occurs.

Noise figure of the test setup is very critical for converter testing. A good grounding technique and short leads must be used to minimize noise problems. A spectrally pure input sinewave which can be achieved with a proper filter must be applied to converters for dynamic performance tests. Usually it is necessary to fabricate a custom printed circuit board must be fabricated to interface with other hardware that provides forcing function. buffering, switching, and measurement capabilities and still provides low noise

Different test algorithms can reduce the effects of noise. A windowing DSP technique must be used for FFT data of SNR measurements for a non-coherent test environment. A window will get rid of the sidelobes around the peak fundamental frequency of a magnitude spectrum and will improve the SNR measurement significantly. A Body window (5-terms) was used to measure the SNR from the magnitude spectrum and it is shown in Figure 5. [7]

Averaging can also be used to reduce noise error. Even though some systematic errors can be removed by calibration, uncertainties can be reduced with averaging techniques. Ten-sweeps were averaged for the SNR measurement of 16-bit ADCs as shown in Figure 5 and the whole averaging process took less than one minute.

VI. Conclusions

Hijl~-speed. high resolution A/D converters are one of the key components in many space electronic systems. Testing such complex devices is a challenging task, especially hardness assurance radiation testing. A simplified testing strategy is crucial for evaluation of these converters within a projected budget and schedule. The test approach must be capable of providing diagnostics of key converter performance and failure modes. Bias conditions must be carefully selected to make sure that the test results are valid for the application

A great deal of effort was expended to test these converters to the limits of their precision and accuracy. However, the results showed that small changes in SNR, INL, and DNL were unimportant until other more easily measured dc parameters exhibited substantial changes. Thus, doing less elaborate tests of dynamic parameters and linearities appears to be adequate, and will save considerable effort and cost, particularly for converters with high resolution Therefore, DC parametric tests with static linearity measurements at major code transitions are recommended as a minimum set of measurements for hardness assurance tests.

The reference voltage is a critical dc parameter' for linearity measurements and for converter functionality, and degradation of internal references was one of the important failure modes of the 14-bit and 16-bit converters. It should be measured along with other dc parameters to characterize the static performance of converters. The direct relationship to linearities with other process related internal devices of converters make the effects of the reference voltage more complex and difficult to understand Use of an external reference generally improved the radiation hardness.

A 16-bit converter with self-calibration was also tested. However, doe to basic monolithic CMOS process fabrication, and the way thal the circuit design was implemented, it actually performed worse than the other two converters which used BiCMOS technology and conventional architectures.

Finally, converters were all affected by dose rates. For two of the converters, radiation failure levels were significantly improved at very low close rates. However, the performance of the third converter was much worse at very low dose rate. The dose rate sensitivity was probably caused by the interplay of hole and interface traps that occurs in MOS device. [8] However, the complex design of these converters and the possibility of many different failure mechanism makes it difficult to interpret the device response at different dose rates.

VI I. References

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